REMARKS

Drawings

Applicant has amended Figures 1 and 2A-2B to designate the legend "Prior Art". Replacement sheets have been included herewith.

Specification

The disclosure has objected to because of the informalities of (Tsi) in paragraph 4 should be (T_{si}). Applicant has amended (Tsi) to (T_{si}).

Claim Rejections - 35 U.S.C. § 102/103

The Examiner has rejected claims 19-21 and 25-26 under 35 U.S.C. § 102(e) as being anticipated by Chau et al (US Patent 6,858,478 filed 2/14/2003). The Examiner has rejected claims 22-24 under 35 U.S.C. § 103(a) as being obvious over Chau et al (US Patent 6,858,478 filed 2/14/2003) in view of Nakajima et al (US Pub. No. 2004/0142567 filed 11/6/2003).

It is Applicants understanding that the cited references fail to teach or render obvious Applicant's invention as claimed in claims 19-21 and 26 as well as new claims 43-47.

35 U.S.C. § 102 Rejections in view of Chau et al.

In claims 19-21 and 26 and new claims 43-52, Applicant teaches and claims a method of forming a semiconductor device which includes forming a semiconductor body having a *"a channel region with a p type conductivity"* and forming a gate electrode which includes a metal film having a *"work function between 3.9 - 4.2 eV"*. It is Applicants understanding that Chau et al. fails to disclose a semiconductor device which includes a semiconductor body with a p type channel region and a gate electrode with a metal film having a work function between 3.9 – 4.2 eV. As such, Chau et al. fails to teach Applicant's invention as claimed in claims 19-21 and 26.

Additionally, with respect to new claims 43-52, Applicant teaches and claims a method of forming a semiconductor device which includes a forming semiconductor body with a channel region having an "n type conductivity" and forming a gate electrode with a metal film having "a work function between 4.9 – 5.2 eV". It is Applicants understanding that Chau et al. fails to disclose forming a semiconductor device which includes an n type semiconductor body and a gate electrode having a metal film with a work function between 4.9 – 5.2 eV. Accordingly, Chau et al. clearly fails to teach Applicant's invention as claimed in new claims 43-47.

35 U.S.C. § 103 Rejections with respect to Chau et al. in view of Nakajima et al.

The subject matter of Chau et al. and the claimed invention at the time the invention was made was owned by the same person or subject to an obligation of assignment to the same person. Accordingly, because Chau et al. constitutes prior art only under 35 U.S.C. § 102(e), Applicant respectfully requests that the Chau reference be removed as a reference under 35 U.S.C. § 103.

Additionally, with respect to Nakajima et al., Nakajima discloses a semiconductor device which includes a NMOS device and a PMOS device. The NMOS and PMOS devices include a gate electrode with a lower polycrystalline silicon film 103, and a W/WN film 104 formed on the silicon film 103, and a silicon nitride film 105 formed on the W/WN film. Nakajima does not disclose a gate electrode having a lower metal film let alone a lower metal film having a work function between 3.9 – 4.2 eV for an n type device or a work function between 4.9 – 5.2 eV for a p type device.

Accordingly, for the above mentioned reasons, it is Applicants understanding that the cited references clearly fails to teach or render obvious Applicant's invention as claimed in claims 19-21 and 26 as well as new claims 43-52.